**BIRLA INSTITUTE OF SCIENCE AND TECHNOLOGY PILANI, HYDERABAD CAMPUS**

**DIGITAL DESIGN LABORATORY (Session 2021-22)**

**Workbook**

**Experiment -6**

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**Complete ID of the student: 2020A7PS2081H**

**Title of Experiment: Dataflow Modelling Implementation of 4-Bit Adder & BCD Adder in Xilinx ISE**

**Problem 1:**

**Implement the 4-bit Adder circuit using Xilinx ISE**

**(Provide proper snapshots and Show the graphical output)**

**Code:**

**Graphical user interface, text, application

Description automatically generated**

**Test Bench:**

**A screenshot of a computer

Description automatically generated**

**A screenshot of a computer

Description automatically generated**

**Graph:**

**A screenshot of a computer

Description automatically generated**

**Problem 2:**

**Implement BCD Adder using 4-bit Adder in Xilinx ISE**

**(Provide proper snapshots and show the graphical output)**

**Code:**

**A screenshot of a computer

Description automatically generated**

**Test Bench:**

**A screenshot of a computer

Description automatically generated**

**A screenshot of a computer

Description automatically generated**

**Graph:**

**A screenshot of a computer

Description automatically generated**

**Problem 3:**

**Implement 4-bit BCD Adder-Subtractor in Xilinx ISE**

**(Provide proper snapshots and show the graphical output)**

**Code:**

**Graphical user interface, text, application

Description automatically generated**

**Test Bench:**

**A screenshot of a computer

Description automatically generated**

**A screenshot of a computer

Description automatically generated**

**A screenshot of a computer

Description automatically generated**

**Graph:**

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